IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) Test switching circuit for a high speed data interface of an integrated circuit comprising:

a plurality of switching transistors which switch in a test mode an integrated termination resistor output stage to an integrated termination resistor input stage, said output stage being coupled to an output pad of said integrated circuit in a data transmission signal path, and said ~~to an integrated termination resistor~~ input stage being coupled to an input pad of said integrated circuit in a data reception signal path,

wherein said plurality of switching transistors are switchable and provide [[for]] a plurality of different internal test signal paths within the test switching circuit between said input pad and said output pad corresponding to a plurality of test operation modes.

2. (Previously Presented) The test switching circuit according to claim 1 wherein the test switching circuit is connected to a configuration register.

3. (Previously Presented) The test switching circuit according to claim 1 wherein the integrated termination resistor output stage is programmable.

4. (Previously Presented) The test switching circuit according to claim 1 wherein the integrated termination resistor input stage is programmable.

5. (Previously Presented) Test switching circuit for a high speed data interface of an integrated circuit comprising switching transistors which switch in a test mode a termination resistor output stage of a data transmission signal path to a termination resistor input stage of a data reception signal path to form an internal feedback test loop within said integrated circuit, wherein the controllable test switching circuit comprises:

a first transistor connected to said termination resistor output stage of the data transmission signal path;

a second transistor connected between said first transistor and a reference potential node;

a third transistor connected between said reference potential node and a sixth transistor;

a fourth transistor connected between said first transistor and a test node;

a fifth transistor connected between said test node and said sixth transistor;

wherein the sixth transistor is connected to said termination resistor input stage of the data reception signal path.

6. (Previously Presented) The test switching circuit according to claim 5 wherein the transistors are formed by MOSFETs.

7. (Previously Presented) The test switching circuit according to claim 6 wherein the gate terminals of the transistors are controlled by control bits stored in said configuration register.

8. (Previously Presented) The test switching circuit according to claim 5 wherein in a normal operation mode of said integrated circuit the first transistor is switched off, the second transistor is switched on, the third transistor is switched on, the fourth transistor is switched off, the fifth transistor is switched off and the sixth transistor is switched off.

9. (Previously Presented) The test switching circuit according to claim 5 wherein in a feedback test mode of said integrated circuit the first transistor is switched on, the second transistor is switched off, the third transistor is switched off, the fourth transistor is switched on, the fifth transistor is switched on and the sixth transistor is switched on.

10. (Previously Presented) The test switching circuit according to claim 5 wherein in a receiver test mode of said integrated circuit the first transistor is switched off, the second transistor is switched off, the third transistor is switched off, the fourth transistor is switched off, the fifth transistor is switched on and the sixth transistor is switched on.

11. (Previously Presented) The test switching circuit according to claim 5 wherein in a transmitter test mode of said integrated circuit the first transistor is

switched on, the second transistor is switched off, the third transistor is switched off, the fourth transistor is switched on, the fifth transistor is switched off and the sixth transistor is switched off.

12. (Previously Presented) The test switching circuit according to claim 5 wherein the controllable test switching circuit is fully differential.

13. (Currently Amended) A high speed data interface within an integrated circuit comprising:

(a) a transmitting signal path for transmitting data via a data transmission line which is connected through an output pad to an integrated termination resistor output stage coupled to the output pad in said data transmission signal path, wherein the integrated termination resistor output stage is provided for adapting the output impedance of said data transmission signal path to a load connected to said transmission data line through the output pad;

(b) a reception data signal path for receiving data via a data reception line, which is connected through an ~~output~~ input pad to an integrated termination resistor input stage coupled to the input pad in said data reception signal path, wherein the integrated termination resistor input stage is provided for adapting the input impedance of said data reception signal path to a load connected to said reception data line through the input pad; and

(c) a controllable test switching circuit comprising a plurality of switching transistors for switching in a test mode the integrated termination resistor output stage to the integrated termination resistor input stage to form an internal feedback test loop within said integrated circuit, wherein said plurality of switching transistors are switchable and provide [[for]] a plurality of different internal test signal paths within the test switching circuit between said input pad and said output pad corresponding to a plurality of test operation modes.

14. (Currently Amended) Integrated circuit having several high speed data interfaces, wherein each high speed data interface comprises:

(a) a transmitting signal path for transmitting data via a data transmission line which is connected through an output pad of said integrated circuit to an integrated termination resistor output stage coupled to the output pad in said data transmission signal path, wherein the termination resistor output stage is provided for adapting the output impedance of said data transmission signal path to a load connected to said transmission data line through the output pad;

(b) a reception data signal path for receiving data via a data reception line, which is connected through an input pad of said integrated circuit to an integrated termination resistor input stage coupled to the input pad in said data reception signal path, wherein the integrated termination resistor input stage is provided for adapting the input impedance of said data reception signal path to a load connected to said reception data line through the input pad; and

(c) a controllable test switching circuit comprising a plurality of switching transistors for switching in a test mode the integrated termination resistor output stage to the integrated termination resistor input stage to form an internal feedback test loop within said integrated circuit, wherein said plurality of switching transistors are switchable and provide [[for]] a plurality of different internal test signal paths within the test switching circuit between said input pad and said output pad corresponding to a plurality of test operation modes.